REMARKS

1. Objection to Specification because of the informality that the pages of the specification are not numbered:

Review of the as-filed application papers sent to the PTO shows the use of page numbers throughout the specification and the claims. It is respectfully requested that the examiner add the page numbers to the patent application, as the lack of page numbers was evidently due to a technical error in the electronic submission process.

2. Objection to Specification because of description of Fig.5:

In the specification, and specifically in the Brief Description of Drawings, the terms first and second embodiment are used consistently to distinguish between two cases of different numbers of code words. Moreover, the description related to Fig.2 does not refer to the process of Fig.2 as the first embodiment.

The applicant argues that the terms "first embodiment" and "second embodiment" used in the manner would not be confusing to one of ordinary skill in the art on reading the disclosure. They would understand that, among other differences, the first embodiment uses an even number of code words while the second embodiment uses an odd number of code words, and that both embodiments are compatible with the process shown in Fig.2.

In view of the above explanation, the applicant requests that the examiner withdraw this rejection.

3. Objection to Claims 1-15 because of informalities in the claim language:

Claims 1-13 cancelled without prejudice or disclaimer to the merits thereof.

In claims 14 and 15 a space has been added between the claim number and the claim, as requested by the examiner. Claim 14 has been revised to better describe the claimed invention. Claim 15 has been made dependent to claim 14, and also revised for clarity.

4. New claims 16-33:

New claims 16-33 are provided to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, to claims 1-13 now cancelled. Claims 16 and 27 are independent. Claims 16-33 are fully supported by the applicant's original claims and disclosure. No new matter is entered.

The applicant requests that the examiner please refer to the following detailed description regarding compliance of claims 16-33 with 35 U.S.C. 112, first paragraph.

Please refer to the paragraph [0005] of applicant's Description of the Prior Art, "In Fig.1, the **bit switch sequence** indicates which bit changes when switching from the current counter value to the next counter value. If this sequence is regarded as an ordered set, in any ordered sub-set of the set, there will be at least one element which appears an odd element of times. This is referred to as **the property of the bit switching sequence** throughout the following description."

It is well-known that a Gray code sequence is characterized by only one bit difference between any two adjacent elements of the sequence. Please refer to Fig. 1, if the bit, which shows the difference between any two adjacent elements of the Gray code sequence, is selected. For example, bit 1 is selected to show the difference of the 1^{st}

(0000) and the 2nd (0001) code word of the Gary code sequence, and bit 2 is selected to show the difference of the 2nd (0001) and the 3rd (0011) code word of the Gary code sequence, which are shown in Fig. 1. All selected bits listed in order can form a sequence. In this specification, this specific sequence is called the <u>bit switch sequence</u>.

For any binary bit, if the value of each bit changes an even number of times, it will be the same as that of the original bit, i.e., 0->1->0, or 1->0->1. Since the Gray code sequence is a binary code sequence, if there is a element which appears an even number of times in a bit switch sequence and a Gray code sequence is determined base on the bit switch sequence, the value of the bit corresponding to the even-time appealing element in the bit switch sequence will be the same as the value of the bit of the initial Gray code of the Gray code sequence. Please refer to Fig. 1 and the Table 1, which is a part of Fig. 1, shown below, taking the first three elements of the bit switch sequence {1,2,1} shown in Fig.1 as an example. The element 1 appears two times, which means that the value of the first bit changes two times in the binary Gray code sequence. Therefore, the value of the first bit of the 1st code word and that of the 4th code word are identical.

<u>Table 1</u>

Binary Gray Code	bit switch sequence
0000	
0001	1
0011	2

0010	1

Furthermore, if all elements appear an even number of times in a ordered sub-set of the bit switch sequence set, there must be two code words in the Gray code subsequence corresponding to this bit switch sequence ordered sub-set that are identical. Please refer to Table 2, which is an example to explain the bit switch sequence property. For example, if there is a bit switch sequence subset {1, 2, 1, 2} and the first code word of Gray code subsequence is (0000), the Gray code subsequence corresponding to this bit switch sequence subset are {(0000), (0001), (0011), (0010), (0000)}. The 1st and the 5th code word are identical.

Table 2

Binary Gray Code	bit switch sequence
0000	
0001	1
0011	2
0010	1
0000	2

Clearly, if there are two code words in any subsequence of a code sequence that are identical, this code sequence cannot be used to count the element because it will cause confusion. Therefore, the bit switch sequence must have the property that all elements in any ordered sub-set of the bit switch sequence set cannot appear an even number of times in this ordered sub-set, that is, there will be at least one element which appears

an odd number of times in this ordered sub-set. In the specification, this property is called the bit switching sequence property.

Based on the above description, if a specific bit switch sequence with the bit switching sequence property is determined in advance, a Gray code sequence can be determined easily without undue experiment.

Please refer to Fig.2, in the embodiment disclosed in the specification, an exponent element M is determined first (in step 10) according to the element of code word of the to-be-determined Gray code sequence (N). Based on the embodiment (starting from paragraph [0024] of the specification), if N=6, then M=3, each code word of the to-be-determined Gray code sequence is a three-bit code. If M is determined, the possible value of each element of the bit switch sequence can be easily determined. The value of each element of the bit switch sequence must be one of {1,2,3}. One of ordinary skill in the art can easily determine a bit switch sequence 7 (2^M-1) elements without undue experiment according to the following two criteria: 1. the value of each element of the bit switch sequence must be one of {1,2,3}; and 2. the bit switch sequence must follow the bit switching sequence property described above.

Please refer to Fig. 3, the full length Gray code sequence has the property that "The full length Gray code sequence is divided into a first half and a second half by an axis of reflection. The first half and the second half are mirror images of one another with the exception of the most significant bit" (lines 9~13, column 4 of US 6,703,950, made of record). Since, the full length Gray code sequence has the above-described

property, the bit switch sequence corresponding to the full length Gray code sequence has the property that "there is a first element which is the middle element of the sequence and which can divide the whole sequence into a first ordered sub-set and a second ordered sub-set which are the same" (paragraph [0025] of applicant's specification). Please refer to Fig.3, which shows the full length 3-bit Gray code sequence and the corresponding bit switch sequence. "Take the first bit switch sequence {1, 2, 1, 3, 1, 2, 1} in Fig.3 as an example. The fourth element '3' is the middle element, by which the whole sequence is divided into two ordered sub-sets {1, 2, 1} which are the same" (paragraph [0025] of applicant's specification).

According to the applicant's disclosure, the second bit switch sequence is determined by deleting elements of the first bit switch sequence. The method to determined the second bit switch sequence through deleting the elements of the first bit switch sequence are described as two examples in the specification.

1. If the number of elements to be deleted is even, the second bit switch sequence can be determined by deleting the same element in the same position from the first ordered sub-set and the second ordered sub-set respectively. In addition, the determined second bit switch sequence must also follow the bit switching sequence property described above (for detailed explanation, please refer to applicant's paragraph [0025]).

2. If the number of elements to be deleted is odd, the second bit switch sequence can be determined by deleting the even number of elements using the method 1 describe above, and then deleting one more element from the remaining elements of the first bit switch sequence. It is also required that the determined second bit switch

sequence must follow the bit switching sequence property described above (for detailed explanation, please refer to applicant's paragraph [0027] to paragraph [0029]).

Thus, it is clear that one of ordinary skill in the art can easily determined the second bit switch sequence through deleting the elements of the first bit switch sequence without undue experiment to meet the criteria described in the embodiments of the applicant's specification. Moreover, if the second bit switch sequence is determined, it is trivial for one of ordinary skill in the art to determine the desired Gray code sequence based on the second bit switch sequence.

Sincerely,

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